In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claims 2, 3, 14, 18 and 26 without prejudice.

1 1. (Currently Amended) A system comprising:

2 a central processing unit (CPU);

3 ~~one or more cache memories, coupled to the CPU, each to store only data for~~

4 ~~loads to be processed by the CPU that have a vitality matching the latency associated~~

5 ~~with the respective cache memory;~~

6 a first cache memory, coupled to the CPU, to store only data for vital loads that

7 are to be immediately processed at the CPU;

8 a second cache memory, coupled to the CPU and the first cache, to store non-vital

9 loads to be processed at the CPU; and

10 a third cache memory, coupled to the CPU and the second cache memory, to store

11 data for semi-vital loads to be processed at the CPU, wherein vital loads update the first

12 cache memory and the second cache memory.

1 2. (Cancelled)

1 3. (Cancelled)

1 4. (Currently Amended) The system of claim 1 ~~3~~ wherein the CPU accesses to the

2 first cache memory, the second cache memory and the third cache memory in parallel.

1 5. (Currently Amended) The system of claim 1 ~~3~~ wherein vital loads are directly

2 assigned to the first cache memory, semi-vital loads are directly assigned to the third

3 cache memory and non-vital loads are directly assigned to the second cache memory.

1 6. (Original) The system of claim 5 wherein the assignment of the loads to the

2 respective caches is performed statically.

1 7. (Original) The system of claim 6 wherein the assignment of the loads is

2 performed at a compiler.

1 8. (Currently Amended) The system of claim 1 ~~3~~ wherein vital loads are to be

2 processed at the CPU within one clock cycle.

1 9. (Original) The system of claim 8 wherein semi-vital loads are to be processed

2 at the CPU within three clock cycles.

1 10. (Original) The system of claim 9 wherein non-vital loads are not to be

2 processed at the CPU for at least four clock cycles.

1 11. (Currently Amended) The system of claim 1 ~~3~~ wherein the first cache memory is

2 a 265B cache and the third cache memory is a 1KB cache.

1 12. (Original) The system of claim 11 wherein the second cache memory is

2 physically larger than the third cache memory.

1   13.   (Currently Amended) The system of claim 1 3 wherein the first cache memory

2   and the third cache memory operate at the same level in cache hierarchy.

1   14.   (Cancelled)

1   15.   (Currently Amended) The system of claim 1 14 wherein semi-vital loads update

2   the third cache memory and the second cache memory.

1   16.   (Original)   The system of claim 15 wherein non-vital loads update the second

2   cache memory.

3   17.   (Currently Amended) A method comprising:

4   identifying load instructions having a first vitality level by filtering out load

5   instructions having a dependence distance greater than a predetermined clock cycle;

6   identifying load instructions having a second vitality level;

7   assigning load instructions having the first vitality level to be stored in a first

8   cache memory; and

9   assigning load instructions having the second vitality level in a second cache

10   memory;

11   identifying load instructions having a third vitality level after identifying load

12   instructions having the first vitality level; and

13   assigning load instructions having the third vitality level to be stored in a third

14   cache memory, wherein vital loads update the first cache memory and the second cache

15   memory.

1   18.   (Cancelled)

1   19.   (Currently Amended) The method of claim 17 ~~18~~ further comprising performing

2   a profile, after identifying the load instructions having the first vitality level, to identify

3   the remaining load instructions that frequently miss in the first cache memory and lines

4   that are not used.

1   20.   (Currently Amended) The method of claim 17 ~~18~~ further comprising performing

2   a profile, after identifying the load instructions having the third vitality level, to identify

3   the remaining load instructions that frequently miss in the third cache memory and lines

4   that are not used.

1   21.   (Currently Amended) A computer system comprising:

2   a central processing unit (CPU);

3   a first cache memory, coupled to the CPU, to store only data for vital loads that

4   are to be immediately processed at the CPU;

5   a second cache memory, coupled to the CPU, to store data for semi-vital loads to

6   be processed at the CPU

7   a third cache memory, coupled to the CPU the first cache memory and the second

8   cache memory, to store non-vital loads to be processed at the CPU, wherein vital loads

9   update the first cache memory and the third cache memory;

10   a chipset coupled to the CPU; and

11   a main memory device coupled to the chipset.

1 22. (Original) The system of claim 21 wherein the CPU accesses to the first

2 cache memory, the second cache memory and the third cache memory in parallel.

1 23. (Original) The system of claim 22 wherein vital loads are directly assigned to

2 the first cache memory, semi-vital loads are directly assigned to the second cache

3 memory and non-vital loads are directly assigned to the third cache memory.

1 24. (Original) The system of claim 23 wherein vital loads are to be processed at

2 the CPU within one clock cycle, the semi-vital loads are to be processed at the CPU

3 within three clock cycles and non-vital loads are not to be processed at the CPU for at

4 least four clock cycles.

1 25. (Original) The system of claim 23 wherein the first cache memory and the

2 second cache memory operate at the same level in cache hierarchy.

1 26. (Cancelled)

1 27. (Currently Amended) The system of claim 21 26 wherein semi-vital loads update

2 the second cache memory and the third cache memory.

1 28. (Original) The system of claim 27 wherein non-vital loads update the third

2 cache memory.